Interconnect Design Tradeoffs for Silicon and Glass Interposers

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Abstract—Interposer technologies offer high density, high performance interconnects for integrated systems resulting in smaller form factors and improved system performance as compared to traditional packages. This paper sheds light on the different design tradeoffs which result from the usage of silicon and glass interposers due to the different material characteristics. The emphasis is on the redistribution layers (RDLs) of the interposer rather than the through silicon vias (TSVs) due to the long length of these wires. Guidelines of designing the interconnects for different design objectives on silicon and glass interposers are presented. Interconnects on glass interposers are more efficient in terms of power dissipation and delay. Conversely, wires on glass interposers suffer from twice as high crosstalk as compared to silicon at minimum pitch. Interconnects on glass interposers exhibit 35% better power-delay product (PDP) than on silicon for fixed pitch at 1.95 \( \mu m \). More importantly, minimum pitch does not result in minimum delay, power dissipation, and crosstalk. The interconnect design parameters that satisfy these objectives under different constraints are different for the two materials. Consequently, the various tradeoffs between area and noise as well as power and delay must be considered in the design process.

I. INTRODUCTION

Interposer technologies have emerged as the demand for interconnection density has significantly increased in high performance devices. This demand towards higher interconnect density on-chip as well as off-chip makes interconnect design a crucial aspect of the design process greatly affecting system performance. Additionally, interposers enable the integration of smaller dies at advanced technology nodes which leads to a higher overall yield as compared to a single die of considerably larger area. Interposer based systems, such as the Xilinx Virtex 7, interconnect multiple dies on a silicon interposer, offering significant power reduction and increase in bandwidth [1]. In addition, miniaturization of packages and systems necessitates the use of high density interposers or packages made of potentially different materials [2].

An interposer based system, often called a 2.5-D system, consists of a passive silicon or glass interposer as a substrate to interconnect multiple active dies. Interposers typically include a number of metal layers which are called redistribution layers, interconnecting the hosted dies. The RDLs are similar to Back End of the Line (BEOL) interconnects. Usually, an older interconnect technology is employed for these layers as compared to the on-chip interconnects of the hosted dies due to the lower resistance and cost [3].

A recent work has shown that interconnects on a silicon interposer have high power efficiency for smaller pitch due to small ground capacitance [4]. However, other important design objectives have not been investigated in [4]. In addition, other materials, such as glass with potential performance benefits need to be explored [2].

In this paper, glass interposers are also considered as an alternative to silicon interposers. In addition, design issues other than power efficiency, such as crosstalk, area, and power-delay product are studied to better ascertain the merits relating to the two types of interposers. A comparison between interconnects for data transmission on glass and silicon interposers at a 65 nm BEOL technology is presented. Power and ground interconnects and the relating noise are not considered in this work. This technology node has also been employed in [1], [4]. Traditional design parameters, such as spacing between wires and width of interconnects are determined for different objectives considering the different electrical properties of both materials. These design parameters are shown to considerably vary between the two materials aiming the same objective and/or design metric.

The paper is organized as follows. In Section II, the technological characteristics and models of both interposer materials are described. In Section III, the physical behavior and performance of interconnects on glass and silicon interposers are investigated and possible tradeoffs are addressed. Design guidelines for interconnects on both materials targeting high density interconnections are offered in Section IV, aiming the reduction of crosstalk, delay, and power. Some conclusions are offered in Section V.

II. INTERCONNECT MODELING ON GLASS AND SILICON INTERPOSERS

In this section, the traits of interposer interconnects are described. A typical example of a system employing interposer technology comprises a processor and memory system as illustrated in Fig. 1. A DDR2 SDRAM is assumed as the memory module, which requires a bandwidth of 400 MT/s [4], [5]. Glass and silicon are used as the two candidate interposer materials. In both cases, the top two metal (Cu) layers are used as RDLs on the interposer. The typical dimensions for global wires according to Predictive Technology Model (PTM) [6] for the chosen technology node are 0.45 \( \mu m \) for space and width, wire thickness is 1.2 \( \mu m \) and dielectric height between metal layers of 0.2 \( \mu m \). Polyimide with \( e_r = 3.5 \) [7], [8] is assumed as the dielectric in the passivation layer for both cases.

Memory and CPU are assumed to be connected with 10 mm long interconnects on the interposer which are modeled as
a distributed interconnect with 100 π-type RLC segments. Self and mutual inductances between wires are also considered, yet at 400 MT/s the interconnects do not exhibit inductive behavior. Consequently, the performance of the interconnects is primarily determined by the RC characteristics of the wires.

Additionally to the wire parasites electrostatic discharge (ESD) capacitors are also included. Microbumps, modeled as RLC elements, are included for each driver and receiver [4]. On-die termination (ODT) is not used. In Fig. 2, the electrical model of three adjacent interconnect wires connecting the previously mentioned CPU and memory circuits, is illustrated.

Closed-form expressions from [9] are utilized to describe the interconnect capacitance. In Fig. 3, the various components of capacitance is shown for both materials. Due to the low permittivity of the glass substrate (e_\text{r_{glass}} = 3.4, [7]), the electric field lines terminate to the neighboring wires in metal layer 7 and the metal layer above. This situation leads to strong coupling capacitance to the adjacent interconnects. Capacitance expressions for parallel lines on one ground plane are employed for interconnects on glass interposer (see left hand side of Fig. 3). Alternatively, the silicon substrate behaves as a ground plane due to the high permittivity of e_\text{r_{sil}} = 11.9 [7]. Hence, capacitance closed-form expressions for parallel lines between two ground planes are used for this structure (see right hand side of Fig. 3). Resistance and inductance closed-form expressions are employed from [6].

IBIS models for the I/O drivers of the CPU [10] and DDR2 SDRAM memory at 400 MT/s [5] are utilized. Clock alignment and data recovery are not considered in the analysis. Hence, the dissipated power is based on the energy supplied by the CPU I/O drivers.

### III. Interconnect Analysis on Glass and Silicon Interposers

The baseline structure for identifying the design tradeoffs is presented in this section. The behavior of glass and silicon interposers is investigated for a 65 nm technology. The minimum pitch for this technology node is 0.9 µm [6]. For high density systems smaller pitches can be required [12].

The interconnects depicted in Fig. 2 are simulated with HSPICE [11] for different switching scenarios. For measuring the power dissipation and the signal delay of the middle interconnect in Fig. 2, wire B is switching while A, C are quiet at the ground level (nominal case). In addition, wire B is silent while A, C are switching together for capturing the voltage noise at the far-end of wire B. In Table I, the RLC characteristics of the interconnects on glass and silicon interposers are listed for minimum pitch.

<table>
<thead>
<tr>
<th>Interconnect element</th>
<th>Glass</th>
<th>Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>40.7 Ω/mm</td>
<td>40.7 Ω/mm</td>
</tr>
<tr>
<td>L</td>
<td>1.98 nH/mm</td>
<td>1.98 nH/mm</td>
</tr>
<tr>
<td>C\text{end}</td>
<td>121.5 pF/mm</td>
<td>222.7 pF/mm</td>
</tr>
<tr>
<td>C\text{coupling}</td>
<td>191.4 pF/mm</td>
<td>105 pF/mm</td>
</tr>
<tr>
<td>C\text{total}</td>
<td>512.9 pF/mm</td>
<td>327.7 pF/mm</td>
</tr>
</tbody>
</table>

Results listed on Table II, show that interconnects of the same length (e.g., 10 mm) on the glass interposer are slightly faster and more power efficient over silicon interposer at minimum pitch. Alternatively, interconnects on glass interposers suffer from higher crosstalk, which can lead to signal integrity problems. Consequently, the same pitch or, alternatively, the same width and space (for fixed pitch) should not be used where different interposers are utilized.

| Interconnect Structure Shown in Fig. 2 for Minimum Interconnect Pitch |
|-------------|----------|----------|
| Glass       | 2.4      | 0.63     | 0.09     |
| Silicon     | 2.3      | 0.7      | 0.3      |

The IBIS models used for the memory I/O receivers at the far-end of the wires recognize logic zero for voltage values between 0 V - 0.65 V and logic one between 1.125 V - 1.8 V [5]. Wires on glass interposers suffer from twice as high crosstalk as compared to silicon as reported in Table II. This effect is more pronounced in interconnects on a glass interposer as the capacitive coupling between adjacent wires is higher than on silicon. In Fig. 4, the peak amplitude noise at the far-end of interconnects on glass and silicon interposers, respectively, is illustrated for varying pitch. Crosstalk noise is mitigated by increasing the space between wires [14]. According to Fig. 4, crosstalk of interconnects on glass interposers decreases by 50% for spacing larger than 1.2 µm as compared to the
upper voltage limit of logic zero ($V_{\text{max, zero}}$). Alternatively, noise on wires on silicon interposers is considered insignificant ($<0.55 \times V_{\text{max, zero}}$) for minimum spacing. Therefore, this behavior of interconnects on glass interposers leads to a design tradeoff between area and noise, in particular, for those systems that require high density interconnections.

Increasing the interconnect pitch also changes the loop inductance of the investigated structure. The overall effect, however, is not significant due to the low speed of DDR2 [5], [13]. For interconnects with faster switching speeds, noise effects from mutual inductance can also contribute considerably to the overall noise [14], further increasing the importance of this area and noise tradeoff.

Propagation delay and power generally form a design tradeoff and power-delay product (PDP) is an efficient way to describe this. The power-delay product of interconnects on glass interposers is significantly lower than silicon as illustrated in Fig. 5. The traits of the interconnects on silicon interposers make PDP to increase twice as fast as compared to glass. As the silicon substrate is modeled as a second ground plane (see Fig. 3), interconnects on silicon interposers have twice as high ground capacitance than on glass interposer. Thus, glass interposers are a better option for systems that target low power and delay assuming a relaxed pitch or, equivalently, relaxed area constraints to avoid crosstalk problems.

Alternatively, for small pitches, which support high density interconnects, especially where spacing between interconnects is less than 1.2 $\mu$m, the PDP for glass increases. This increase is due to the increase in coupling capacitance reducing the PDP difference between the two types of the interposers as depicted in Fig. 5 for $W$ and $S$ smaller than 1 $\mu$m. Therefore, a design tradeoff between PDP and area is formed for high density interconnects on glass interposers. As illustrated in Fig. 4, predominantly for spacing larger than 1.2 $\mu$m, crosstalk noise drops considerably for interconnects on glass interposers. Hence, for relaxed pitch, ground capacitance is the primary capacitance component. As this component is lower for glass than silicon, the PDP for glass interposers does not increase with wire width as fast as in silicon interposers.

Based on these observations, interconnects on glass and silicon interposers behave differently for disparate objectives, such as crosstalk and PDP. Moreover, this behavior varies for different area constraints. Therefore, determining the appropriate design parameters, such as spacing and width for high density designs is an important task as the resulting performance can vary considerably between the different interposers.

**IV. Design Guidelines**

In this section, design guidelines are proposed for interconnects on glass and silicon interposers. Different area constraints, such as large pitches and high density designs, are considered.

As mentioned in the previous section, for large spacing, the coupling capacitance of adjacent interconnects on a glass interposer is greatly reduced. Hence, ground capacitance becomes dominant. Therefore, interconnect width is the most important design parameter for both materials and large pitches. For the investigated 65 nm technology node, this guideline applies for pitches larger than 2 $\mu$m. Wires on a silicon interposer exhibit twice as high ground capacitance as compared to glass structure. Consequently, increasing the wire width on a silicon interposer leads to considerably higher PDP than in glass interposer (see Fig. 5). Thus, wider interconnects can be employed on glass interposers as compared to silicon. Consequently, glass interposers are a superior choice for low-power and delay constrained designs where area constraints are relaxed.

Alternatively, designs with strict area constraints require different design guidelines due to the different behavior of interconnects. For systems with stringent power and area budget, minimum interconnect width has to be applied to both materials so that the capacitance to the ground is minimum. However, for small pitches, coupling capacitance increases. This situation is more severe for glass. Therefore, for fixed pitch, minimum interconnect width and maximum space should be selected, particularly for glass interposers. The results listed on Table II for minimum pitch and in columns 3 and 4 of Table III for width 0.45 $\mu$m, demonstrate this situation.

Increasing the width of wires is a usual means to reduce delay. However, for interconnects on glass interposer the effect of crosstalk on delay is not negligible, in particular, for the
### TABLE III. SIMULATIONS FOR INTERCONNECTS ON GLASS AND SILICON INTERPOSERS FOR DIFFERENT DESIGN OBJECTIVES.

<table>
<thead>
<tr>
<th>Fixed pitch = 1.95 (\mu m)</th>
<th>Power [mW]</th>
<th>Delay [ns]</th>
<th>PDP [mJ]</th>
<th>Noise [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Space [(\mu m)]</td>
<td>Width [(\mu m)]</td>
<td>Glass</td>
<td>Silicon</td>
<td>Glass</td>
</tr>
<tr>
<td>1.50</td>
<td>0.45</td>
<td>1.883 (min)</td>
<td>2.064 (min)</td>
<td>0.4470</td>
</tr>
<tr>
<td>1.35</td>
<td>0.60</td>
<td>1.967</td>
<td>2.248</td>
<td>0.3867</td>
</tr>
<tr>
<td>1.20</td>
<td>0.75</td>
<td>2.099</td>
<td>2.432</td>
<td>0.3463</td>
</tr>
<tr>
<td>1.05</td>
<td>0.90</td>
<td>2.215</td>
<td>2.595</td>
<td>0.3287</td>
</tr>
<tr>
<td>0.90</td>
<td>1.05</td>
<td>2.329</td>
<td>2.786</td>
<td>0.3238 (min)</td>
</tr>
<tr>
<td>0.75</td>
<td>1.20</td>
<td>2.510</td>
<td>2.984</td>
<td>0.3276</td>
</tr>
<tr>
<td>0.60</td>
<td>1.35</td>
<td>2.674</td>
<td>3.178</td>
<td>0.3256</td>
</tr>
<tr>
<td>0.45</td>
<td>1.50</td>
<td>2.896</td>
<td>3.467</td>
<td>0.3509</td>
</tr>
</tbody>
</table>

worst case scenario where A and C wires switch opposite to B (see Fig. 2). In this scenario, the interconnect delay measured for the design parameters resulting to the minimum delay in the nominal case, increases by 26% for the glass and 7% for the silicon structure, respectively. As listed in Table III, different width and space have to be employed for interconnects on glass and silicon interposers such that the delay is minimum. The reduction of delay for interconnects on glass interposers from minimum pitch \((S = W = 0.45 \text{ \(\mu m\)})\) to 1.95 \(\mu m\) pitch, where \(S = 1.5 \text{ \(\mu m\)}, W = 0.45 \text{ \(\mu m\)}\) and \(S = 0.45 \text{ \(\mu m\)}, W = 1.5 \text{ \(\mu m\)}\), is 30% and 44%, respectively. For wires on silicon interposers the decrease in delay is 18% and 48%. Thus, simply increasing the width for a fixed pitch does not necessarily benefit delay. Hence, increasing wire spacing on glass interposers is a more efficient way to reduce delay so that the contribution of the coupling capacitance to the delay decreases. Alternatively, reducing interconnect delay on silicon interposers, is primarily achieved by increasing the wire width, which reduces the interconnect resistance.

For the power-delay product the previous guidelines have to be combined. As listed in Table III, the minimum PDP for interconnects on both glass and silicon interposers results for the same design parameters\(^1\) \((S = 1.2 \text{ \(\mu m\)} \text{ and } W = 0.75 \text{ \(\mu m\)})\). This result emphasizes the different behavior of interconnects on glass and silicon interposers. The PDP for interconnects on silicon interposers is minimum for very small widths e.g., \(W = 0.75 \text{ \(\mu m\)}\), due to the low ground capacitance which is the primary capacitive component. Conversely, large spacing \(S = 1.2 \text{ \(\mu m\)}\), results in minimum PDP for glass interposers due to the reduction of capacitive coupling between adjacent interconnects. Furthermore, the difference of the minimum PDP between the two materials in Table III, decreases from 35% to 9% for the worst case scenario, mainly due to higher effect of coupling capacitance on interconnects on glass interposers than on silicon interposers.

Finally, interconnects on glass interposers are more prone to crosstalk noise than on silicon. Therefore, for voltage noise specifications around 0.25 V, interconnects on glass interposers have to be placed farther apart \((S = 1.5 \text{ \(\mu m\)})\). This results in a non-negligible increase in PDP by 16% as compared to the minimum PDP for interconnects on glass interposers. Thus, the difference of PDP between silicon and glass decreases by 10%. In spite of this increase, however, the PDP for glass remains lower than on silicon in the nominal case. Small pitches are applicable for glass interposers, as long as the crosstalk constraints are not over-restrictive (i.e., \(V_{\text{max\_noise}} < 0.14 \times V_{\text{dd}}\)).

\(^1\)Slightly different values can result for a finer sizing step.

### V. CONCLUSIONS

In this study, design guidelines for interconnects on glass and silicon interposers that satisfy area, power, delay, and crosstalk constraints are determined for a 65 nm technology node. Interconnects on glass interposers are a superior alternative to silicon interposers in terms of power and latency. On the contrary, interconnects on glass are more prone to crosstalk effects than on silicon. This situation requires a different treatment for sizing the interconnects as there is a tradeoff between area and noise for the glass interposers. Furthermore, the minimum pitch does not result to minimum power, delay, and crosstalk. Finally, increasing the wire width on a silicon interposer leads to higher power consumption than on glass for the same width. Consequently, glass interposers are a better solution for low-power systems under the same latency constraints.

### REFERENCES


