Memory Management

The Operating System Memory Manager

The Memory Hierarchy (1999!)

Storage Type	Access Time	Capacity	Managed by
Registers	1 nS	100 to 1K	compiler
?	2-10 nS		CPU hardware
Main Memory		100M to 1G	
Disk Storage			

The Address Space

- Machine instructions:

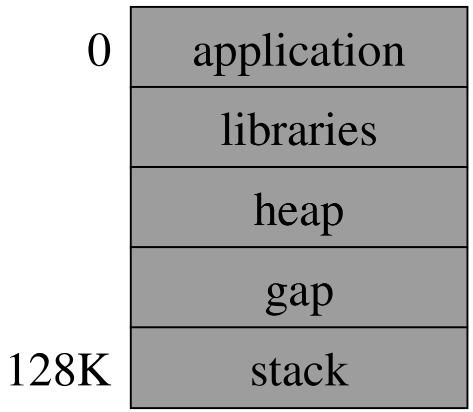
  load (r1)

  jump (r3)

- Address width is:
  - 32 bits in Pentium
  - 64 bits in Alpha, Itanium, SPARC-V9
- Addresses need *binding* to locations before use

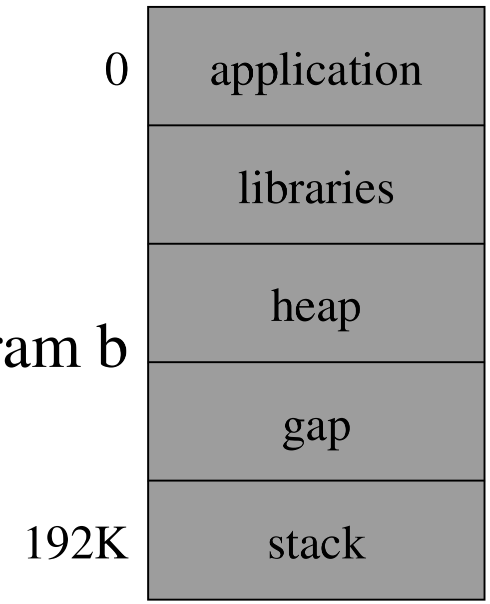
Address Binding Requirement

- Compiler allocates addresses within module
- Linker allocates addresses within program



Program a

Program b



Adress Binding in Action

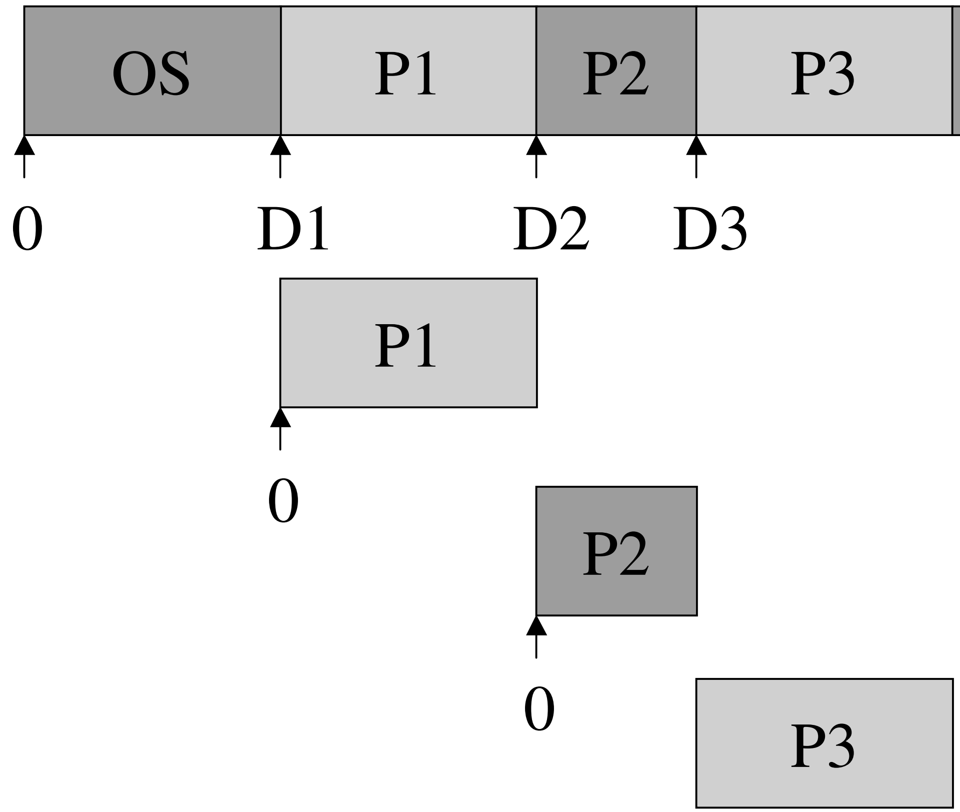
Option (a): fixup addresses when program is loaded

- But …

Option (b): use Dynamic Address Translation

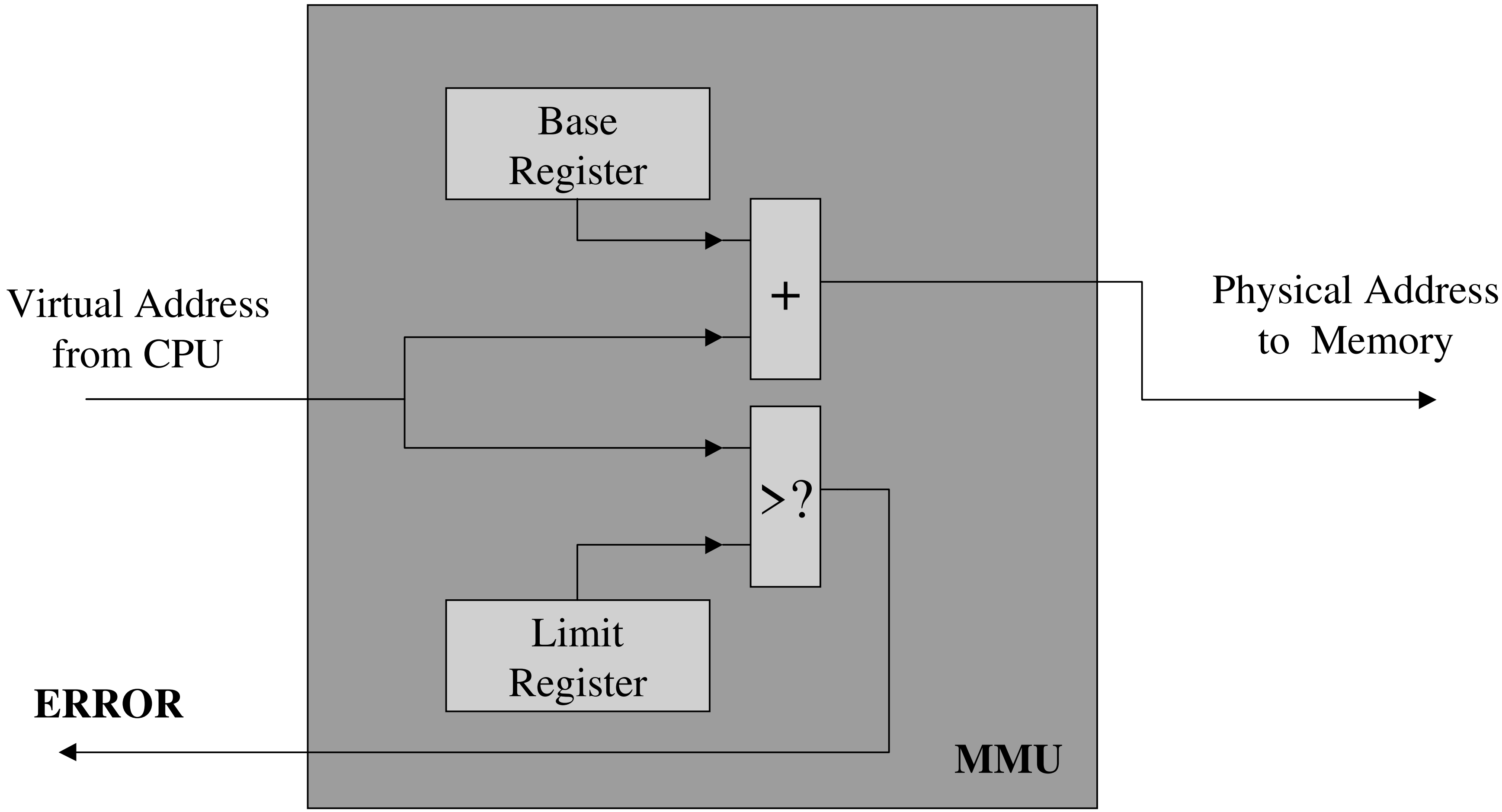
- Translate *program* addresses into *main memory* addresses during execution
- Use different translations for different programs

Dynamic Translation: Datum scheme



n.b. *Fragmentation*

Protection:


Base
Register
+
Virtual Address
from CPU
Physical Address
to Memory
>?
Limit
Register
ERROR
MMU

Towards Sharing?