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THE EDSAC

PART II

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4. Components of the EDSAC - Tactical Functions.

The above description of the principal components is intended to show the relation between the strategic functions of various parts of the machine. Attention will now be given to the manner of operation of individual components in order to show how they fulfil their respective functions. It is first necessary to outline the various basic elements, which are combined in different ways to form operational components of the machine.

4.1. Basic Elements.

Delay Lines. The use of ultrasonic delay lines appears at present to be the most satisfactory method of achieving circulatory storage of a pulse train or of providing a delay, of $\frac{1}{2}$ M/C or more, in a pulse train. For shorter delays, of the order of 1 or 2 μsec., a simple electrical delay line is used. This consists of a group of π sections, each comprising a coil of 350 μH inductance bounded by two 50 pF condensers. Ten such units in cascade provide a delay of about 2 μsec.

For non-repetitive delays - i.e. delays of single pulses - of the order of $\frac{1}{2}$ to 1 M/C, a phantastron circuit (described elsewhere *) is used.

Gates. A gate consists of two diodes with a common anode load resistor. The inputs to the cathodes, and the output are normally through cathode followers, but in units such as Decoders, containing a considerable number of gates, cathode followers are used only at the input and output of the whole unit. The circuit is described in greater detail by Wilkes and Renwick (loc. cit.).

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*Williams, F.C. and Moody, N.F., Journ.I.E.E., 93. III A, No.7., p.1188, 1946.

A triple gate is similar to the normal gate, but has three, instead of two, diodes.

Gate circuits are used also for inhibiting the passage of pulses, or for reversing (i.e. interchanging 0's with 1's).

Flip-flops. In general, flip-flops are required to maintain a given state for only a short time, of the order of a millisecond or less. It is therefore possible to use condensers in the input and output circuits, thus simplifying the associated circuit design very considerably. The basic circuit is shown in Fig. 5. The flip-flop is normally in the 'reset' state (i.e. V_1 cut off), unless set by a positive pulse. It is then reset either by a 'reset' pulse, or by the lapse of some milliseconds, after which it returns naturally to the 'reset' state.

The positive output passes to a cathode follower, which provides also a negative output, if required, from an anode load resistor.

Adding Diodes. It is frequently necessary to permit the passage in a single lead, of a pulse occurring in any one or more of a group of possible sources. This is done by applying each input lead to the anode of a diode, the cathodes all being connected through a common load resistance to earth, to form the output.

4.2. Memory.

The Memory has been fully described elsewhere. However, it has associated with it a number of auxiliary components, of which the most important are the Main Buses and the Distributing Unit I. The Main Buses will be dealt with in § 4.45.

The Distributing Unit I is used to provide a route to or from the

Memory tank specified in the Tank Number Decoder. The unit consists of a number of cathode followers through which the Decoder output is routed, and both positive and negative e.m.fs. provided, where required, at the appropriate destinations. The detailed requirements of the Distributing Unit I will become apparent when considering the Tank Number Decoder in § 4.46.

4.3. Input.

In order to appreciate the significance of the input sequences, it is necessary to give some attention to the method of programming a problem. In order that the machine should start computing, it is required to have available in Memory the orders and numbers (in binary form) needed in the solution. The use of initial input and synthesis orders for this purpose was described in § 3.22.

The transfer of synthesis orders uses only the normal processes of the machine, and the input equipment therefore consists of the two major components - the Tape Input and the Initial Input - which require separate description.

4.31. Tape Input.

The Tape Input may be subdivided into -

(a) The Tape Reader.

(b) The Addition Unit.

(c) The Inhibition Unit.

The Tape Reader is used, on receipt of an I - order, to scan the next row of holes in the punched tape and to set relays to represent the data in static electrical form. The Addition Unit converts these data into

dynamic form, as a train of pulses of suitable form for transfer to Memory. The Inhibition Unit serves to delay the operation of the machine if an input order is received before the previous input order has extracted the required data from the tape.

The carrying out of an I - order takes place in two stages. In the first stage, the tape is read and the data stored in the Addition Unit. The second stage does not take place until receipt of the next I - order, which causes the data already stored in the Addition Unit to be transferred to Memory, at the same time initiating the reading of the next row of holes in the tape.

The Tape Reader consists of standard teleprinter equipment with minor modifications. Associated with it is a camshaft which, by means of a special clutch, is caused to rotate once when an I - order is received. The action of the camshaft causes the row of holes in the tape to be 'read', the data being stored in the relays and converted to pulses in the Addition Unit. At the same time, the I - order causes the machine to proceed with Stage II, i.e. the finding of coincidence for transfer to Memory of the number already stored in the Addition Unit in the previous I - order. Owing to the comparatively slow speed of the electromechanical components this transfer takes place, and the Addition Unit is cleared, before the camshaft has had time to transfer new data from the tape to the Addition Unit.

As soon as the transfer to Memory has taken place, the machine is permitted to proceed with its next sequence of operations, while the camshaft is still carrying out the remainder of its function. However, if while it is doing so, a new I - order is received, the sequence of operations must be

suspended to allow the previous I - order to be completed before proceeding with the new one. The Inhibition Unit is used for this purpose.

The Inhibition Unit consists essentially of two gates, known as G_4 and G_2, which provide alternative routes for the '1' pulse to the Sequence Control Tank. G_4 is normally open, but on receipt of an I - order, it is immediately closed for the period required to find coincidence. At the same time, G_2 is opened to allow one pulse to pass, and is immediately closed again. The circuits associated with G_2 are such that G_2 will not open again until the camshaft has made almost a complete rotation and the data on the tape transferred to the Addition Unit.

The passing of a single pulse through G_2 allows the machine to proceed with the next operations in sequence, G_4 being reopened and providing a route for the addition of 1's. However, if, before the camshaft has completed its rotation, another I - order is received, G_4 is again closed and there is now no alternative route through G_2. Thus the addition of 1's is inhibited. Coincidence will, however, take place once every major cycle and will transfer the contents of the Addition Unit to Memory. Each such transfer will supersede the previous one, and this process will continue until the whole of the appropriate tape data have been transferred to the Addition Unit, so that eventually the correct data will appear in Memory superseding a series of incorrect data which have been transferred during the period of inhibition.

At this stage, the presence of the new I - order ensures, through a suitable circuit, that the camshaft will make a further rotation, and at the same time, the inhibition of the passage of 1's ceases, so that the

machine may again proceed with its sequence of operations while the camshaft rotates and carries out the pending I - order.

By means of the above device, it is possible to ensure that the slowness of the input mechanism will not limit the speed of the machine in carrying out normal operations, but will prevent interference with an I - order by another I - order following it in quick succession. When no further I - order is present, the camshaft comes to rest.

4.32. Initial Input.

The Initial Input provides the Memory with the orders necessary to initiate the transfer to Memory of the contents of the tape. As mentioned before, these contents commence with the synthesis orders which control the transfer of the input data appropriate to the problem under investigation.

The initial input orders are stored in banks of uniselectors, each bank containing 8 'columns', each of 25 switch positions. Since more than 25 switching operations are required, two sets of uniselector banks are used, the operation of the second set being initiated by the final operation of the first.

Each initial input order contains 17 digits, and 2 further 'columns' are required for auxiliary switching operations. Thus, 19 columns are required, and are supplied by 3 banks of 8 columns each. For the two sets, therefore, 6 banks of uniselectors are provided.

Each column in the uniselector assembly is wired to the appropriate digit pulse, P_{19} to P_{35} being used for this purpose.

The first operation in the Initial Input is to set up the initial conditions for operation. These conditions require that:

(a) The S.C.T. must be cleared, leaving its contents as 00000.

(b) A reversing switch provides that the normal Stage I operation - transfer of an order from Memory - is reversed, and becomes a transfer into Memory. (It is convenient to use the Stage I sequence as a means of carrying out the Initial Input).

(c) The first initial order must go to Memory Position 00000.

(d) The Initial Input must take over from the M.C.U. the function of adding 1's to the S.C.T., and must also provide end pulses to the M.C.U. at the conclusion of each transfer. The Initial Input is provided with a '1 - emitting unit', which provides 1o pulses for addition to the S.C.T.

(e) The stimulating pulse from the M.C.U., which normally initiates Stage II, must be suppressed, so as to confine the sequence to Stage I.

Having established these conditions, the Initial Input data are transferred, order by order, to Memory through the operation of the uniselectors. Finally, the S.C.T. must be cleared so that the M.C.U. can take control by initiating the carrying out of the Initial Input orders, which are now stored in Memory. In doing so, the usual '1' is not added to the S.C.T., since the sequence of orders must start from Memory position 00000, and not 00001.

4.4. Control Section.

The general method of control has been outlined in § 3.3. Certain components of the Control Section consist of tanks, flashing units, etc. which have been described in § 3.3., and the following paragraphs will be

devoted to a more detailed description of the Coincidence Unit, the Sequence Control Tank and the Main Control Unit, and their inter-relation with each other and with other parts of the machine.

4.41. Coincidence Unit.

The Coincidence Unit is shown schematically in Fig. 6. Its purpose is to emit a coincidence gating e.m.f. under the following conditions:

(a) It must be connected to either the Order Tank or Sequence Control Tank, and thus be 'conscious' of the particular M/C or half M/C in which the required number appears in Memory. This information is available in pulses O_1 to O_6 of the order.

(b) It must have received a stimulating pulse from the Main Control Unit.

and(c) Coincidence must have been achieved between O_2 to O_6 of the order and the corresponding pulses of the Counter Tank. The gating e.m.f. is emitted at the first D_0 or D_{19} after coincidence has been achieved.

At first sight, this appears to indicate a lag between coincidence and the carrying out of the order. However, the position within a major cycle must be considered in terms of a purely arbitrary zero, and is related to the way in which the number concerned was first transferred from Input to Memory. The transfer to Memory is achieved through the Coincidence Unit under precisely the same conditions as a transfer from the Memory. It is therefore clear that the conditions for achieving coincidence are valid provided only that the Counter Tank has operated without interruption from the time the number was first transferred to Memory.

The receipt of a stimulating pulse, at time D_0 from the M.C.U. sets the flip-flop F/F_3, providing an e.m.f. for the triple gate G_8. This gate

will therefore allow a D_0 or D_{18} pulse to pass, provided that F/F_1 is set, and this occurs only when coincidence has been found. This implies that F/F_1 must be in the 'set' state at the instant a D_0 or D_{18} pulse is received by the triple gate. It is clear that the arrival of one or other of those pulses will set F/F_1 after $\frac{1}{2}$ p.i delay due to DL 1. The condition then is that F/F_1 should remain set until the next D_0 or D_{18} is received. Now the action of the system $G_1 - 4$ is such that if, during the period D_2 to D_6, coincidence fails to occur in any one digit, a pulse passes through the adding diodes a_2 and resets F/F_1, thus inhibiting the emission of the coincidence gate. If, however, after the receipt of a stimulating pulse, complete coincidence in digits D_2 to D_6 is found between the order and the contents of the Counter Tank, then no resetting pulse is passed to F/F_1, which therefore remains set until the next D_0 or D_{18}, which accordingly passes through G_8 and sets F/F_4, emitting a coincidence gating e.m.f. The same pulse, delayed for 1 M/C in DL_5, is passed through G_5 in the form of a resetting pulse R. The R-pulse is used to signify to the M.C.U. that coincidence has been found and that it may now proceed to the next operation. The delay line DL_5 is introduced to ensure that the R - pulse is not emitted until sufficient time has elapsed for the transfer from Memory of the number, either short or long, to have taken place.

The above procedure ensures that the coincidence gate is stimulated at the correct instant as determined by the establishment of coincidence, and that the R - pulse is emitted 1 M/C later. It remains only to ensure that the coincidence gate is inhibited at the proper instant, whether the number sought in Memory occupies a full M/C or either the first or second

half M/C. If the number occupies a full M/C or the second half M/C, the gate must clearly be inhibited at the next D_0, but if the first half M/C, the inhibiting pulse must be the next D_{18}. This is achieved by means of the gate G_6, which admits D_{18} as an inhibiting pulse only if the appropriate e.m.f. F_1, specifying a short number, has been emitted by the Half-cycle Flashing Unit.

The positive e.m.f. emitted by F/F_4 is used to stimulate the coincidence gate. At the same time, a negative e.m.f. is emitted, in order to clear the Order Tank and to avoid unwanted coincidence. This occurs whenever coincidence is found, both in Stage I, and in Stage II where applicable. The clearing of the Order Tank is unnecessary in Stage II, but does not affect the operation in any way and is therefore allowed to proceed, so as to avoid unnecessary complication.

The delay line ML_4 and gate G_7 are used only to isolate F/F_4 from unnecessary resetting pulses.

4.42. Sequence Control Tank.

The S.C.T. stores the Memory position of the order to be carried out and thus holds the data contained in O_1 to O_{12} which are used, at the appropriate time, to determine the behaviour of the Tank No. and Half-cycle Flashing Units and the Coincidence Unit.

Normally, the S.C.T. commences with the Memory position 0, and proceeds by the addition of one at the conclusion of the carrying out of each order, so that the orders are selected in numerical sequence. The addition of one is achieved by the emission of a pulse from the M.C.U. to the half-adder associated with the S.C.T.

In the case of a conditional transfer order requiring the breaking of the normal sequence, a gating e.m.f. is emitted by the M.C.U. which allows the contents of the Order Tank to be transferred to the S.C.T., and to replace the data held there. At the same time, the addition of one is suppressed for the next operation.

4.43. Main Control Unit.

It is now possible to describe the supervisory functions of the M.C.U. in its relation to the other components of the Control Section and the Memory and Computer. The M.C.U. is shown schematically in Fig. 7.

On the receipt of an end pulse, or of any other signal indicating the completion of the carrying out of an order or of a 'Start' pulse, the M.C.U. first initiates Stage I, the extraction of the next order from Memory. When this has been done it receives a resetting pulse R_1, from the Coincidence Unit. This causes the M.C.U. to initiate Stage II, the carrying out of the order, the completion of which may be indicated by either an end pulse (from the Computer), a pulse R_2 from the Coincidence Unit (when this unit is required in Stage II) or a Dv(D) (conditional transfer) pulse. The M.C.U. then proceeds to the next Stage I operation.

The M.C.U. has therefore to discriminate between an R_1 pulse, for initiating Stage II, and the other types of pulse, including R_2. Since R_1 and R_2 both come from the same source in the Coincidence Unit, a special device is used for separating them within the M.C.U. This device is based on the fact that an end pulse, or any pulse acting as an end pulse, causes the emission of a gating e.m.f. g_{12}. An R - pulse which is received while g_{12} is present must be an R_1 pulse. Thus, the gate C_3 is opened by g_{12} and

only R_1 can pass through it. Having done so, R_1 stops g_{12} and causes an e.m.f. g_{13} to be emitted. This in turn opens G_4, providing a route for R_2, which is no longer able to pass through G_3. Thus R_1 and R_2 travel by separate routes.

The tactical purpose of the M.C.U. is as follows:

Stage I.

(a) On receipt of end pulse, or equivalent, it emits the gating e.m.f. g_{12}, to provide the necessary routes for Stage I, namely: S.C.T. to C.U. and to Tank No. and Half-cycle Flashing Units. Order Tank to Main Output Bus.

(b) it emits a stimulating pulse to the C.U., to enable it to seek coincidence.

Stage II.

(a) On receipt of R_1, it emits g_{13}, which provides a route from the Order Tank to the Coincidence Unit and all Flashing Units.

(b) it emits a stimulating pulse to the Computer, and, in operations requiring it, to the C.U.

(c) In the case of a sign pulse following a Conditional Transfer Order, it emits a gating e.m.f. connecting the Order Tank to the S.C.T.

These functions are carried out as follows:

An end pulse, or equivalent, occurring at D_0 or D_{18}, passes through the normally open gate G_2 and sets F/F_2, causing g_{12} to be emitted. At the same time, it sets F/F_1 which permits the next D_0 to pass through G_1 and G_8 as a stimulating pulse, F/F_1 being immediately reset.

On receipt of R_1, F/F_2 is reset, inhibiting g_{12}, and F/F_3 is set, providing g_{13}. At the same time F/F_1 is again set, and the next D_0 provides the stimulating pulse for Stage II.

In operations requiring the C.U., an R_2 pulse is received and passed on to the Computer. It also provides through G_6, for the addition of 1 to the S.C.T.

In the case of orders T, T^1, I, O or M, the arrival of R_2 signifies the end of the operation, and the gate G_5, stimulated by an e.m.f. from the Order Coder, permits R_2 to be applied to G_2 as an end pulse.

A sign pulse, Dv(D), occurring at D_0 following a Conditional Transfer Order, sets F/F_4 which emits both positive and negative gating e.m.fs. to the input and clear gates of the S.C.T. The input of the S.C.T. is normally connected to the Order Tank, so that the e.m.fs. emitted by F/F_4 cause the S.C.T. to be cleared and to receive the contents of the Order Tank. At the same time, the addition of 1 to the S.C.T. is inhibited by the gate G_6.

The M.C.U. also provides facilities for stopping the machine, e.g. for checking by suppression of end pulses through gate G_2, or to cause continued repetition of an order for testing purposes, by suppressing the addition of 1 to the S.C.T.

It is important to ensure that no stimulating pulse is emitted when the order does not require the use of the C.U. The gate G_8 is included to inhibit the passage of the pulse under those conditions. G_8 is actuated by an e.m.f. from the Order Coder when the order requires a stimulating pulse in Stage II. A stimulating pulse is required always in Stage I, and use is made of the fact that at the commencement of Stage I, the Order Tank has been

cleared and the digits stored in it are therefore all zero. The order code for the digits 0_{13} to 0_{17} does not include the sequence 00000, which may therefore be used as an order for Stage I, and therefore as a condition for the emission of the stimulating pulse.

4.44. Order Tank.

The Order Tank is used to store the portion of an order which designates the position of a M/C in a particular Memory Tank. This is necessary, in addition to the static storage of the tank number and the operational part of the order, to enable the C.U. to find coincidence. The Order Tank is a mercury delay tank having $\frac{1}{2}$ M/C delay. Only the digits 0_1 to 0_6 require storage to establish coincidence, but the whole order is stored, in order to keep it available for the setting up of the appropriate flashing units.

4.45. Transfer Unit and Main Buses.

The normal method of transferring a number from one component to another is through the output gate of the first component to the Main Output Bus, then through the Transfer Unit to the Main Input Bus, and finally through the input gate of the second component. Thus in general, the main Output Bus is connected to all output gates, and the Main Input Bus to all input gates. To initiate an operation, one input and one output gate are opened, together with all necessary auxiliary gates.

The Transfer Unit is used to ensure that all short numbers and all orders occur in the correct half M/C. For example, a number in Memory, occurring in a first half M/C, must be delayed by one half M/C before entering the Accumulator. Conversely, for a transfer to a first half M/C