represented by D_2 to D_6 in the Counter Tank reaches equality with the appropriate digits (specifying the M/C) in the S.C.T., the C.U. emits a coincidence gating e.m.f., which opens the route from Memory to the Order Tank, to which the required order is transferred.

As soon as the order has been brought from Memory, it is possible to initiate Stage II, namely the carrying out of the order. The functions of the Supervisory Control in Stage II are essentially the same as in Stage I, but are modified according to the nature of the order obtained in Stage I. For example, the order may not involve the finding of a number in Memory, in which case the establishment of Coincidence is not required. If, however, the order includes a Memory position, the part O_2 to O_6 is stored in the Order Tank, which plays the same part in establishing coincidence as the Sequence Control Tank plays in Stage I. Attention will be paid later to the variations in the procedure for Stage II, according to the type of order to be carried out.

3.33. Temporary Storage and Routing.

The carrying out of an order normally involves the transfer of a number from a given Memory position, which involves the selection of a given minor cycle in a particular tank. It is therefore necessary to store the order in dynamic form, so as to provide the necessary data to the Coincidence Unit. This storage is provided by the 'Order Tank', which is similar in principle to a Memory Tank, but has a shorter mercury column, providing only a half minor cycle delay. Thus the order circulates twice every minor cycle, and is readily available for the establishment of coincidence.

However, the dynamic storage of an order is in itself insufficient,

since the operational part of the order must be able to hold open the various routes (to the specified Memory tank, etc.) for the indefinite period, up to one major cycle, required to establish coincidence. The order must therefore be stored statically as well as dynamically. This is achieved by means of flashing units. The operational part of the order is stored in the Order Flashing Unit, and the numerical part (Memory position) is stored in the Tank Number and Half-cycle Flashing Units.

A flashing unit comprises a series of flip-flop circuits, each of which may be regarded as having two stable states, at least for sufficient time for their function to be carried out. When actuated by a train of pulses representing an order, or part of an order, each flip-flop takes up one or other of its stable states, to represent the appropriate digit in the order. The condition of the flip-flops indicates a route appropriate to the particular order. For example, the Tank Number Flashing Unit indicates the number of the tank designated in the order to which it is required to provide a circuit in order to carry out the order.

3.34. Decoders.

The routes indicated by the flashing units are provided by means of 'decoders', which, when actuated by the flip-flops, provide gating e.m.fs. where required to allow pulse trains to pass as required.

3.35. Order Coder.

In the case of the Tank Number Decoder, the routing is quite straightforward, since the tank numbers are coded in binary form. However, the carrying out of an order involves a number of alternative routes, depending on the nature of the order, and a unit known as the 'Order Coder'

is required to interpret the binary data set up in the Order Decoder as an actual route.

3.36. Alignment of Numbers and Orders.

A long number occupies a fixed place in a minor cycle, and the binary point is thus in a fixed position, so that operations such as addition can be carried out directly. However, a short number may occupy the first or second half of a M/C, and in the former case, the binary point occurs between pulses p_{15} and p_{16}, whilst in the latter, and in a long number, it occurs between p_{33} and p_{34}. Thus if a number appears in the first half of a M/C, it must be shifted one half M/C to the left before any arithmetical operation is carried out.

Conversely, if a short number resulting from an arithmetical operation (and therefore with its binary point properly aligned) is to be stored in the first half M/C of a Memory position, it must be shifted one half M/C to the right before storage.

A similar shift is required when transferring an order to the first half M/C of a Memory position.

The appropriate shifts are achieved by the 'Transfer Unit', which contains a half minor cycle delay tank, together with gates controlled by the 'Half-cycle Flashing Unit'. The latter unit stores, in static form, the order data specifying the position in the M/C, viz. O_1 (long or short number), and O_2 (first or second half M/C). The Half-cycle Flashing Unit is also required to provide the data necessary for the Coincidence Unit to establish coincidence when transferring a number to or from Memory.

3.37. Conditional Transfer.

Although the Conditional Transfer cannot be regarded in any sense as a unit of the machine, it is so important a function in the operation of the machine that it merits a general description at this stage. The conditional transfer order is used to allow the machine to determine whether a pre-determined condition has been met, and if so, to change to a new, pre-determined sequence of operations. In particular, the order D(n) requires that the machine should carry on with the carrying out of orders in sequence if the number contained in the Accumulator is negative, but that, if it is positive or zero, the next order should come from memory position n. Provision is made also for the use of the order $D^1(n)$, which operates in a similar manner, but with a positive total in the Accumulator as the criterion for carrying on in sequence.

In carrying out repetitive sequences, it is useful to note that the numerical part of an order may be subjected to arithmetical operations. For example, the first sequence may include an order relating to memory position k, but the following sequences may require the same order to be applied successively to the numbers in positions (k + 1), (k + 2), etc. This may be achieved by including, at the appropriate time in each sequence, the addition of 1 to the particular order, so that the order stored in one memory position will suffice to deal with a succession of numbers in different memory positions.

3.4. The Computer.

The Computer is the section where the basic arithmetical operations are carried out. These include addition, complementing, collation,

multiplication and shifting. The whole section is controlled by the Computer Control Unit. Subtraction is achieved by complementing and adding. There is no provision at present for division, which can usually be avoided by proper programming, but it is possible that a dividing unit will be provided in due course.

The results of operations are stored in the 'Accumulator', which consists of two tanks of nearly 2 M/C total delay. Since numbers, each numerically less than 2, may be added successively into the Accumulator, it is possible, without proper programming, to overload the Accumulator - i.e. to bring the number in it beyond the limits ± 2. To show when this has occurred, an additional sign digit, identical with and adjoining the normal sign digit, is included with every number added into the Accumulator. The total in the Accumulator will therefore also have an additional sign digit at Po, and it is easily shown that the two sign digits will be identical only if the number n in the Accumulator is such that $-2 \leqslant n < 2$.
The two sign digits will be different if these limits have been exceeded, and the machine is automatically stopped and an alarm given.

The following example illustrates this point.

	Sign digits		binary point
No. in Accumulator	00	1	01101 = 1.40625
No. added to Accumulator	00	0	11110 = 0.9375
True total	1	0	01011 > 2
Total shown in Accumulator	01	0	01011

The Accumulator has a delay of 68 pulse intervals (i.e. 2 M/C - 4 pulse intervals). A further delay of 4 pulse intervals is introduced in the circuits associated with the Accumulator tank, making a total delay of

2 M/C. These circuits comprise two half-adders (to be described later), the 'Accumulator Shifting Unit' (A.S.U.) and the 'Complementer-Collater'. The A.S.U. introduces normally a delay of 2 pulse intervals, which may be altered either to 1 or 3, as a means of achieving a right or left shift, respectively, of one pulse interval every 2 M/C, i.e. a shift of one digit for each circulation of the number in the Accumulator.

3.41. Addition.

The Accumulator, Adder (= two half-adders) and A.S.U. form a closed circulation system. Addition is carried out by introducing the addend, as a train of pulses into the Adder. The Adder operates in the following way.

The half-adder shown schematically in Fig. 4(a) comprises an electronic circuit, which receives simultaneously two trains of pulses. Its output also consists of two trains of pulses, such that one of the output trains represents the sum of individual digits in the numbers represented by the input trains, neglecting the 'carry' digit, while the other output train represents the carry. The relation between input and output is shown in the following table, in which the digits 1 and 0 represent the presence or absence of a pulse, respectively.

INPUT		OUTPUT	
A	B	'Sum'	'Carry'
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

If a 'carry' pulse, when present, is delayed by one pulse interval and fed back into one of the inputs, for example, input B, it will clearly be added in the correct place for carrying out an addition. However, the delayed pulse may coincide with a pulse in B, in which case it will be neglected, since the Adder cannot discriminate between a single pulse and two pulses from different sources in the one input. Thus the simple half-adder shown in Fig. 4(a), can only add correctly provided that it is impossible for a delayed pulse in the feedback to coincide with a pulse in input B. This condition is met when the input B is a pulse in the least significant place only, and thus the half-adder may be used as a counter of events which cannot occur twice within the delay time of the associated tank. Thus, half-adders are used in conjunction with the Sequence Control Tank and Counter Tank in the Control Section (see § 3.32).

Consider now the case of a half-adder without feedback. Since there can be only two input numbers, it is clear that the delayed carry digit D, can be 1 only when the previous 'sum' digit C, is 0. If both outputs are fed directly into another half-adder with feedback as shown in Fig. 4(b), it is clear that a pulse in the feedback cannot possibly coincide with a pulse in the delayed 'carry' output from the first half-adder, and so the output E will represent the true sum A + B.

3.42. Complementing.

Negative numbers are represented as complements, with the appropriate sign digit. A complement may thus be formed from the number itself by inverting every digit in the number and adding one. This is obviously the same as inverting every digit after the first 1, the number being read from

right to left, as shown in § 2.

The 'Complementer' consists simply of a normally open gate, which is replaced by a reverse gate immediately after the first pulse has passed.

3.43. Collation.

Collation is the process of multiplying each digit of a number by the corresponding digit of another number. Thus, in the output, the digit 1 appears only when the corresponding digits in both numbers are 1.

To achieve this, it is necessary only to provide a gate, which admits a pulse from one input to the output, only if there is simultaneously a pulse in the other input.

Collation provides a means of removing unwanted digits, for example in the process of selection of data from the input tape.

3.44. Multiplication.

Multiplication is carried out by successive additions of the multiplicand, with appropriate shifts, into the Accumulator. For this purpose, two tanks - the Multiplier Tank and the Multiplicand Tank - and a Multiplicand Shifting Unit are used.

On receipt of an M - order, the multiplier is transferred from Memory to the Multiplier Tank. On receipt of the following N - order, the Multiplicand is first transferred from Memory to the Multiplicand Tank. The sequence of addition of partial products is then initiated and controlled by the Computer Control Unit.

The least significant digit of the Multiplier, if 1, allows a pulse D x (M) to be sent to the C.C.U., which emits a gating e.m.f., allowing the contents of the Multiplicand Tank to be transferred to the Accumulator.

If the digit is 0, the gating e.m.f. is not emitted. The Multiplicand Shifting Unit then causes the Multiplicand to be shifted one place to the left, and the process is repeated for the second digit, and so on.

Special precautions have to be taken in the case of a negative multiplicand. Since the Accumulator has a delay of nearly 2 M/C, and the partial products are added in at various positions in the Accumulator, the most significant digit in the Multiplicand will not in general correspond with the most significant digit in the Accumulator. When the partial product is negative, it is therefore necessary to add in a series of 1's to fill the Accumulator, so that the partial product as added to the Accumulator, represents the proper complement. For example:

Multiplicand	11	0101
Multiplier	01	1001
	111	11110101
Partial products	111	10101
	111	0101
Product	110	11101101

If the Multiplier is negative, the partial product for the sign digit in the Multiplier must pass through the Complementer before addition to the Accumulator.

3.45. Shift Orders.

The orders R(n) and L(n) apply to the shifting of a number in the Accumulator n places to the right or left ($1 \leqslant n \leqslant 10$). This is equivalent to dividing or multiplying by 2^n. The value of n is represented by the same group of pulses (C_1 to C_{10}) as in the orders involving a Memory position, but is not coded in binary form. Instead, a single pulse occurs at C_n, the

nine other pulses being absent. The Accumulator Shifting Unit is used to carry out these orders.

3.46. The Accumulator.

The Accumulator Tank with its associated circuits, provides a delay of 2 M/C, and is divided physically into two parts, I and II. Accumulator I provides a delay of 1 M/C, and Accumulator II, 1 M/C minus 4 pulse intervals. The purpose of the division is to allow a number to be extracted in any M/C, instead of waiting till every second M/C.

The delay of 2 M/C comprises 72 pulse intervals, which at the beginning of every second M/C, provide for two sign digits and the 34 most significant digits in Accumulator I, and the less significant digits in Accumulator II and the circuit. A T- or T'-order causes the transfer to Memory of the number in Accumulator I.

The 'Accumulator Warning Unit' is used to stop the machine and ring an alarm, either on receipt of a Z(3) order, or if the Accumulator is overloaded, as indicated by inequality of the two sign digits.

3.5. Output.

The Output mechanism consists essentially of normal teleprinter components, the coding being appropriately modified. The presentation of results in the Output may be either in the form of punched tape or of printed data. The exact nature of the presentation is specified in the programming of the problem, and the necessary printing instructions are included as part of the series of orders applied through the Input to Memory.

Numbers may be presented in the Output in decimal form by means of a rather simpler process than the decimal-binary conversion described in § 3.24.

In the case of a positive number, the four digits to the left of the binary point in the Accumulator (viz. P_{34}, P_{35}, P_0, P_1) are transferred to Memory. (For the first transfer, P_{35}, P_0, and P_1 are all zero). The remainder is multiplied by 0101, i.e. 10×2^{-3}, and shifted three places to the left, the digits in the above four positions being again transferred to Memory. This process is continued until the number has been completely transferred. It is easily shown that the groups of digits transferred to Memory represent the decimal digits of the number.
