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Cambridge University Mathematical Laboratory.

THE EDSAC.

This Report describes the purpose and construction of the EDSAC (Electronic Delay Storage Automatic Calculator) as it exists either as actual equipment or in the design stage, at the time of writing (May 1948).

The Report is intended only for use within the Mathematical Laboratory, and is in no sense a publication of the Laboratory. It will no doubt require modification from time to time as the construction of the machine proceeds, and components which have not been fully constructed or designed are described only in general principle.

THE EDSAC.

1. Introduction.

2. Representation of Numbers and Orders.

3. Components of the EDSAC - strategic functions.

   3.1. Memory.

   3.2. Input.

      3.21. Tape input.
      3.22. Initial Input.
      3.23. Orders.
      3.24. Coding and conversion.

   3.3. Control Section.

      3.31. Components.
      3.32. Supervisory control.
      3.33. Temporary storage and routing.
      3.34. Decoders.
      3.35. Order Coder.
      3.36. Alignment of numbers and orders.
      3.37. Conditional transfer.

   3.4. Computer.

      3.41. Addition.
      3.42. Complementing.
      3.43. Collation.
      3.44. Multiplication.
      3.45. Shift orders.
      3.46. The Accumulator.

   3.5. Output.

1. Introduction.

The application of electronic devices to computing machines and instruments is already widely established, but it is generally accepted that the term 'electronic' machine should be applied only to those which use electronic means to carry out the actual mathematical functions, rather than simply to control the operation of relays or counters. At the present time (May 1948), one electronic machine only - the ENIAC, at the Moore School of Electrical Engineering in Pennsylvania - is known to be in full operation, although a number of others are projected, or are under construction.

The ENIAC fulfils satisfactorily the purpose for which it was designed, but its limitations for general computing work have resulted in a modified approach to the design of further machines. In particular, there has been a marked trend towards (a) a larger memory capacity, and (b) the use of the binary, rather than the decimal, scale for computing processes. An increased memory capacity will obviously lead to greater flexibility and scope. The use of the binary scale has certain advantages which result mainly from the fact that electric or electronic circuits can deal more readily with a variable which has only two stable states than with one which has ten.

A number of electronic binary digital machines are being developed in the U.S.A., in Great Britain and elsewhere. This report deals only with the machine known as the EDSAC (Electronic Delay Storage Automatic Calculator), which is under construction in the Mathematical Laboratory of the University

of Cambridge, and no attempt is made to compare the methods and devices used in the EDSAC with those used in other machines.

The EDSAC will have initially a memory capacity equivalent to that required for 512 ten-decimal numbers (i.e. numbers comprising 34 binary digits). The numbers or orders will be represented by trains of electrical pulses, each pulse lasting approximately 0.9 μsec, the repetition frequency being 500 kc/s. Each pulse has an approximately square wave form, the amplitude being of the order of 18 volts. The presence or absence of a pulse will represent respectively the digit 1 or 0. Although the machine will carry out all internal operations in the binary scale, conversions from the decimal to the binary scale, or vice versa, will take place in the machine, so that, from the point of view of the operator, the use of the binary scale need not be taken as a serious limitation to its convenience of operation.

To facilitate a description of the machine, it is desirable to consider first the ways in which numbers will be represented, stored and transferred from one storage device to another.

2. Representation of numbers and orders.

In general, every number or order is represented by a train of pulses, an order occupying 18 pulse intervals, and a number either 18 or 36 pulse intervals, according to whether the number is of five or ten decimal digits. The period occupied by a ten-digit number (i.e., 36 pulse intervals) is known as a 'minor cycle' (M/C), the length of which is approximately 72 μsec. The digits are represented in succession,

starting from the least significant, i.e. the right-hand digit, and are followed by a 'sign' digit and a blank. The sign digit is 0 for a positive number and 1 for a negative number.

Numbers containing ten and five decimal digits will be referred to as 'long' and 'short' numbers, respectively.

The position of the binary point is between the sign digit and the highest significant digit (i.e. between the 35th and 34th digit position for a long number, and between the 17th and 16th digit position for a short number).

Negative numbers are represented as complements, a unit sign digit indicating the quantity -1, to which the remainder of the number is added.

It should be noted that it is common practice in some centres to represent a binary number on paper with the least significant figure on the left. However, the convention adopted in relation to the EDSAC is similar to that used in ordinary decimal notation. The left-hand digit denotes the sign, the next is the most significant digit, followed by the remaining digits in descending order of significance. Thus:

$$01101 \text{ represents } + (1 + 2^{-1} + 2^{-3})$$

$$\text{and } 1101101 \text{ represents } -2 + (1 + 2^{-2} + 2^{-3} + 2^{-5})$$

A binary point may be inserted after the first digit, but it is not represented physically in a pulse train.

It is clear from the above that every number, n, represented in the machine must be such that $-1 \leq n < 2$.

It is important to note that in forming a complement, all digits, starting from the right, are identical with those in the original number up

to and including the first '1'. The remaining digits, including the sign digit, are reversed.

For example:

Original number: 01.1001 1000

Complement: 10.0110 1000 ←

Precautions are taken to see that in processes such as addition, the binary points are properly aligned.

The pulses contained in a minor cycle are designated p_0, p_1, p_2.....p_{35}. The digits of a long number are represented by the pulses p_1 to p_{34}, p_{35} being the sign digit and p_0 a blank. A short number may occupy either the first or second half of a minor cycle, and is represented by either p_1 to p_{16}, sign digit p_{17}, (p_0 blank), or p_{19} to p_{34}, sign digit p_{35}, (p_{18} blank).

A system similar to that used for representing numbers is used also for orders. An order occupies a half minor cycle and is normally in two parts, the first, or numerical, part representing a 'memory position' and the second, or operative, part representing the nature of the order, suitably coded.

A single train of pulses, as described above, provides a transient representation of a number or order, and is useful only in performing a single operation, such as a transfer from one position to another. In general, however, it is necessary to retain numbers or orders in the machine, either for the short time required to allow a single mathematical operation to be completed, or for a longer time when the number is required at various stages in the solution of a problem. Provision must also be made for the

temporary retention of an order in static form whilst it is being carried out. To meet the former requirement a 'memory unit' is required, which will enable a number, in pulse form, to be repeated at regular intervals, and so to be available for use at any time. The retention of orders in static form is accomplished by 'flashing units' which translate the train of pulses representing an order into a temporary form which enables the order to be carried out.

Experience has shown that the memory unit is of such fundamental importance that it must be considered as the basic unit on which the whole design of the machine depends. It is therefore desirable to describe the operation of the Memory before proceeding to a general description of the machine as a whole.

3. Components of the EDSAC - strategic functions.

The principal components of the EDSAC are as follows:

(a) Memory.

(b) Input.

(c) Control section.

(d) Computer.

(e) Output.

3. 1. Memory.

Various types of memory unit have been described elsewhere, and include those depending on electrostatic, ultrasonic, magnetic or other phenomena. The memory unit used in the EDSAC consist of a number of ultrasonic delay tanks, and has recently been described in detail. *

* Wilkes, M.V. and Renwick, W., Electronic Engineering, 20, p.208, July, 1948.

Superficially, each tank consists of a mercury-filled steel tube of 1 inch external diameter, lying horizontally between two end blocks approximately 5 ft. 4 in. apart. The tanks are arranged in 'batteries', each containing sixteen tanks.

A large memory capacity is desirable, and the EDSAC will have initially capacity for 512 long numbers. In order to avoid an excessive number of tanks with their associated control gear, each memory tank is designed to deal with 16 numbers, and thus 32 tanks are required.

The requirement for each tank is to admit in succession 16 pulse trains, each of one minor cycle duration, and to provide for their constant repetition in sequence. Thus the tank must provide an output, identical in form with the input, but delayed by 16 M/C (i.e. about 1.15 millisec.), the output being fed back into the input to initiate the next series of pulse trains.

In principle the tank is essentially a pulse delay unit which provides a delay of exactly 16 M/C to each pulse received and then returns it to the input of the tank for further circulation. Each tank thus provides a self-contained system in which a series of pulses, having once been introduced from an external source, will continue to circulate with a repetition frequency of about 870 c/s, one complete cycle of operations being known as a 'major cycle' and containing 16 x 36 (= 576) pulse intervals, or 16 minor cycles. The major cycle is illustrated diagramatically in fig. 1.

The memory tank takes the form of a tube of mercury terminated at each end by a piezo-electric crystal. Each incoming pulse is used to

modulate a carrier wave of frequency 13.5 Mc/s, and the modulated signal is applied to the crystal at the input end of the tank. The electrical pulse is thus converted into a mechanical pulse of ultrasonic frequency, which travels to the other end of the tank, where the receiving crystal converts it again into an electrical pulse. The length of the tank is designed to provide a delay of exactly one major cycle.

In order to avoid the progressive distortion in wave-form which would occur due to successive passages through the tank, a special device is used to 'rejuvenate' the pulse after each passage. This device makes use of 'clock pulses', which are the basic timing pulses for the whole machine.

Clock pulses are simply a succession of digit pulses at regular intervals of 2 micro-sec., and are used as a master timing device. The mercury-filled tanks have an appreciable temperature coefficient of velocity, and thus of delay, and it is of course essential that the timing of pulses should be uniform throughout the machine. This could be achieved by ensuring a uniform and constant temperature in all tanks, but it is sufficient if the temperature of all tanks is equal - not necessarily constant - if the repetition frequency of the clock pulse generator is also controlled by a tank at the same temperature. This is the method to be adopted, and will ensure uniformity of pulses throughout, even though their frequency may vary appreciably from time to time. It is therefore customary to discuss the timing of events in terms of major or minor cycles, or pulse intervals, rather than in terms of milliseconds or microseconds.

The outcoming pulse from the tank is not fed directly back to the

input, but, instead, is used to 'gate' an undistorted clock pulse. Thus the input pulses to the tank are always undistorted, and the only distortion in the output pulse is that due to a single passage through the tank. It should be noted that in addition to limiting distortion, this device also limits any progressive drift in the timing of pulses. It is therefore used in various parts of the machine where time lags are likely to appear in electronic circuits, and where it is necessary to 'tidy up' the output pulses.

The 32 tanks are assembled in 'batteries' of 16, and each tank has associated with it a control panel, known as Panel 1/, which, in addition to provision for input and output, contains also the terminals necessary for input, output and 'clear' gating waveforms.

The transfer of a number from Memory is carried out by applying a suitable gating e.m.f. to the output gate. This does not, however, remove the number from the tank, where it remains in circulation until another number is required to replace it. In this case, the new number is admitted through the input gate, and the clear gate is closed for the corresponding interval to inhibit circulation of the original number.

For the transfer of data from one position to another two 'buses' are provided. These are known as the 'Main Input Bus' and 'Main Output Bus', and provide routes to and from various components of the machine. The actual transfer of the data is controlled by gates in the respective components, and takes place according to the orders stored in the machine.

Since each memory tank contains the information stored in 16 minor cycles, the transfer of a number involves the selection not only of a

route (by means of gates), but also of the actual M/C of half M/C within the major cycle stored in the particular memory tank. Thus the operation of gates must be controlled not only in a geographical sense, but also precisely in time. This operation is thus analogous to that of a stroboscope, except that it occurs once only for any particular transfer. It is carried out by means of a 'Coincidence Unit'.

Apart from the 16 M/C delay tank used in the Memory, delay tanks of various lengths are used for temporary storage and for other purposes elsewhere in the machine.

Mention was made earlier of the need for static storage of orders, as opposed to the dynamic storage which is achieved by circulation through the delay tanks. Static storage is required, for example, to enable a route to be kept open, by means of gates, during the process of 'finding' a number in a memory tank and transferring it to another part of the machine. The 'Flashing Unit', which achieves this purpose, consists of a series of 'flip-flop' circuits, so arranged that when actuated by a train of pulses, they will assume an electrical configuration such that each flip-flop, by its 'on' or 'off' state, will represent one digit of the order, and will maintain its state for sufficient time for the order to be carried out. The flashing unit is normally reset automatically before each operation.

The above description is sufficient to enable the general method of operation of the machine to be understood. A more detailed description of the memory and storage devices will be given later.

3.1. Input.

The Input section consists of two parts - the Tape Input and the Initial Input.

3.21. Tape Input.

The Tape Input provides a means for introducing into the Memory the whole of the instructions and numerical data required for the solution of a problem. These data are prepared in the form of punched tape, and the operation of punching the tape can be regarded as a physical interpretation of the 'programming' of the problem, and thus represents the stage where human planning gives place to purely automatic physical operations. From this stage onwards, the machine operates automatically and presents the solution on punched tape or in printed form. It should be noted that the act of punching numerical data on the input is done in decimal notation and the output may be similarly presented.

In the sequence of operations associated with the input of data to Memory, all numbers are converted from decimal to binary form. The whole of the sequence of input operations may take place before the solution of the problem proceeds, or may, by suitable programming, occur at various stages of the solution.

3.22. Initial Input.

The transfer of orders from Input to Memory is in itself a series of operations which requires the existence of orders in Memory to allow it to take place. These initial orders may be applied by some form of mechanical switching, and a number of banks of uniselectors provide a very suitable method. However, the number of operations involved is rather

large and would require an excessive number of contacts in the uniselectors if the whole process were to be carried out by this method. It is more convenient to use the normal processes of the machine as far as possible in the initial transfer of orders to Memory.

Provision is therefore made for this initial transfer to be carried out in two stages. The first is the transfer of a set of standard orders, known as initial input orders, to Memory, by means of uniselectors and associated equipment, known as the 'Initial Input'. These orders enable the machine, through its normal processes, to transfer to Memory from the input tape a standard series of 'synthesis orders', which provide for the remainder of the input process to be carried out.

Although the initial input and synthesis orders are normally of standard form, the occasion may arise for variation of the synthesis orders to suit a particular problem. This may be left to the discretion of the programmer, who may prefer to punch a special series of synthesis orders on the input tape, rather than use the standard set of synthesis orders.

3.23. Orders.

At this stage, the description will be helped by an outline of the types of order with which the machine will deal. They are designated by symbols, which normally comprise a numerical and an operational part. The numerical part usually indicates a position in Memory, which is coded in the following way.

Order pulses are designated O_n, the pulses O_1 to O_{12} comprising the numerical part, and thus serving to indicate:

(a) Which of the 32 memory tanks contains the number to be operated on.

(b) Which of the 16 minor cycles in that tank.

(c) Whether a short or long number.

and (d) If a short number, whether the first or second half M/C.

The pulse 0_1, if present, denotes a long number.

The pulse 0_2, if present, denotes the second half M/C.
if absent, denotes the first half M/C.

The pulses 0_3 to 0_6 specify the M/C, in binary notation.

The pulses 0_7 to 0_{11} specify the tank number in binary notation.

The pulse 0_{12} is a spare.

The pulses 0_{13} to 0_{17} form the operational part of the order.

The coding of this part is quite arbitrary within certain broad limitations, and at the time of writing, the code has not yet been specified. The types of order are as follows:

A(n) = Add. Transfer number from Memory position n, and add into Accumulator. (The Accumulator is a tank which contains the result of operations in the Computer).

S(n) = Subtract. Transfer number from position n, and subtract from total in Accumulator.

M(n) = Prelude to multiplication or collation. Transfer from position n to Multiplier Tank in Computer.

C(m) = Collate. To collate is to multiply the corresponding digits of two numbers, e.g.

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011011101
000111111
000011101
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C(m) is the order to collate the number in Memory position m with the number already in the Multiplier Tank, and add the result into the Accumulator.

N(m) = Multiply. Multiply the number in position m by the number in the Multiplier Tank and add product into Accumulator.

N'(m) = as in N(m), but subtract from total in Accumulator.

T(n) = Transfer from Accumulator to Memory position n, and clear Accumulator.

T'(n) = As in T(n), without clearing Accumulator.

I(n) = Input. Read next row of holes on Input Tape and put result into Memory position n.

O(n) = Output. Punch first 4 binary digits of number in position n, on Output Tape.

D(n) = Conditional Transfer Order (C.T.O.). Examine sign of number in Accumulator. If negative, carry on with orders in normal sequence. If positive or zero, transfer control to that specified in Memory position n.

R(n) = Right Shift. Shift contents of Accumulator n places to right ($1 \leqslant n \leqslant 10$).

L(n) = Left Shift. As in R(n).

Z(1) = Round off number in Accumulator to 34 binary digits (i.e. add 1 to 35th digit).

Z(2) = Round off number in Accumulator to 16 binary digits.

Z(3) = Stop machine and ring alarm bell.

3.24. Coding and Conversion.

The coding of orders is arbitrary, within the limits of standard teleprinter tape, which provides for five holes (or spaces) abreast. A hole and a space represent the digits 1 and 0 respectively. Use is not made of the combinations 11111 and 00000, the former being reserved for overprinting errors, while the latter is indistinguishable from blank tape. Orders are transferred to Memory in groups of four or five digits at a time.

In the case of numbers, the coding occurs in two stages. The first stage takes place in the punching of the tape, in which decimal notation is automatically transferred to coded decimal notation. Each row of holes represents a decimal digit of the number, expressed in binary form, thus requiring only four of the five possible positions. The digits (i.e. rows of holes) are then transferred, in descending order of significance, to the least significant places in the required memory position. Before each successive addition of a decimal digit, the total already in the Accumulator is shifted three places to the left to make room for the incoming digit. This is equivalent to multiplying the total by 8, whereas the factor should be 10. Thus, before making the shift, the total already in the Memory position must be multiplied by 1.25, which, in binary notation, is 01.01. For example, if the number, expressed in decimal notation, is $a_0, a_1, a_2 \ldots\ldots\ldots a_9$, its true value is $a_0 + a_1 \times 10^{-1} + a_2 \times 10^{-2} + \ldots\ldots + a_9 \times 10^{-9}$. The digit a_0 is first placed in coded decimal form, in the

four lowest positions in the Memory position, so that it appears in Memory as $a_o \times 2^{-33}$.

When multiplied by 01.01, and shifted three places to the left, it becomes $a_o \times 10 \times 2^{-33}$, expressed in full binary form. When this process has been carried out ten times, the value of this digit in Memory becomes $a_o \times 10^{10} \times 2^{-33}$.

Similarly, the digit a_1 alone, shifted nine times, would appear as $a_1 \times 10^9 \times 2^{-33}$. Thus, when the whole number has been transferred, the total in the Memory position will be:

$$10^{10} \times 2^{-33} \ (a_o + a_1 \times 10^{-1} + a_2 \times 10^{-2} + \ldots\ldots + a_9 \times 10^{-9}).$$

This total is then multiplied by $10^{-10} \times 2^{33}$, and the product will represent the input number in true binary form. The multipliers used during the coding process, namely 10×2^{-3} and $10^{-10} \times 2^{33}$, are respectively 1.25 and approximately 0.86. They therefore comply with the requirement that all numbers used in the machine must be less than 2, but the need for the multiplier 0.86 requires that no number numerically greater than 1.72 may be transferred from Input to Memory, since otherwise, the Accumulator would become overloaded before the final multiplication takes place.

A similar process takes place in the case of a short number, with appropriate modifications in detail.

3.3. Control Section.

The Control Section is the group of components which control the sequence of operations of the machine and provide the detailed 'instructions' for carrying them out. In particular, it normally subdivides each operation

into two stages, as follows:

Stage I involves the determination of the next order in the computing sequence, the extraction of that order from Memory and its temporary storage in a decoded form - i.e. the form in which the carrying out of the order will automatically follow the extraction from Memory (or elsewhere) of the number on which it is to operate.

Stage II involves the extraction of the number concerned and the completion of the sequence of operations prepared for it in Stage I. This is followed by the emission of an 'end pulse', or its equivalent, which initiates Stage I of the next sequence, and so on.

Although the Control Section initiates and controls the various numerical operations, the actual timing of the operations is regulated by clock pulses, or by pulses directly synchronized with them. In this sense, the Control Section may perhaps be best regarded as a preselector which controls the passage of pulses between various parts of the machine.

In addition to clock pulses, which are emitted regularly at approximately 2 μsec. intervals, a series of 'digit pulses' is also available, each digit pulse being repeated every minor cycle at the same position in the cycle. They are designated Dn, where n specifies the number of the pulse in the M/C. Fig. 2 illustrates the timing of the D pulses.

The various sequences of operations will be described in relation to block schematic diagrams, in which the following colour code will be used where required:

Green = Number or order pulse train.

Blue = Periodic pulses (e.g. clock, digit, M/C).

Violet = Timing pulses, not periodic (e.g. end pulses, etc.)

Black = Negative going D.C. potential (e.g. gating wave-form.)

Red = Positive going D.C. potential.

3.31. Components of the Control Section.

The principal components of the Control Section are as follows:

(a) For supervisory control:

(i) Main Control Unit (M.C.U.)

(ii) Sequence Control Tank (S.C.T.) with half-adder.

(iii) Coincidence Unit (C.U.), permanently connected to

(iv) Counter Tank with half-adder.

(b) For temporary storage and routing:

(i) Order Tank.

(ii) Tank Number Flashing Unit.

(iii) Tank Number Decoders.

(iv) Order Flashing Unit.

(v) Order Decoders.

(vi) Order Coder.

(c) For alignment of numbers and orders:

(i) Half Cycle Flashing Unit.

(ii) Transfer Unit.

In Fig. 3, which illustrates the components of the Control Section, the interconnecting lines are schematic and are intended only to indicate the relation between units. The colour code is accordingly omitted.

3.32. Supervisory Control.

The M.C.U. is stimulated by either:

(a) a 'start' pulse, at the beginning of a solution.

(b) and 'end' pulse, which signifies the end of an operation.

or (c) a 'conditional transfer' pulse, known as Dv(D).

On receipt of one or other of these pulses, the M.C.U. initiates Stage I of the next order. This involves 'finding' the order in Memory, and for this purpose, it emits a gating e.m.f., which connects the Sequence Control Tank to certain Flashing Units and to the Coincidence Unit.

The S.C.T. is essentially a device for counting operations, and therefore stores the Memory position of the next order to be carried out, since the orders are normally held in successive positions in Memory, with certain exceptions which will appear later. The Tank Number Flashing Unit selects and provides a route to the appropriate tank, while the C.U. serves to select the precise position in that tank. In this respect, 'position' must be interpreted as position in a time scale - a 'Memory position' is specified by the number of the tank together with the 'position' in the tank, since each tank contains in circulation the contents of 16 minor cycles. The 'Counter Tank' with its 'half-adder' simply serves to count minor cycles, the five least significant digits being sufficient to specify any particular minor cycle within the major cycle of the Memory tanks. The half-adder is used to add one to the number in the Counter Tank at the beginning of each M/C.

As soon as the C.U. receives a stimulating pulse from the M.C.U., it is ready to 'seek coincidence'. This means that as soon as the number